

TM4614C

N+P-Channel Enhancement Mode Mosfet

General Description

- Low $R_{DS(ON)}$
- RoHS and Halogen-Free Compliant

Applications

- Load switch
- PWM

Product Summary

N Channel

$V_{DS} = 40V, I_D = 6.3A$

$R_{DS(ON)} = 30m\Omega$ (typ.) @ $V_{GS} = 10V$

P Channel

$V_{DS} = -40V, I_D = -5.9A$

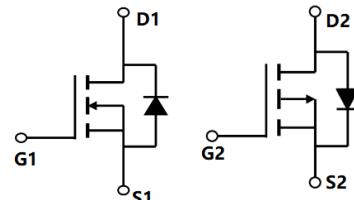
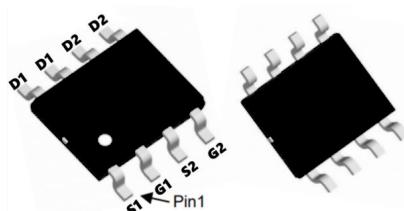
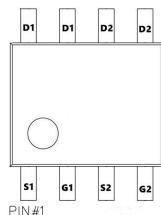
$R_{DS(ON)} = 68m\Omega$ (typ.) @ $V_{GS} = -10V$



100% UIS Tested

100% R_g Tested

S:SOP-8L



Marking: 4614C

Absolute Maximum Ratings ($T_c = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
V_{DS}	Drain-Source Voltage	40	-40	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	6.3	-5.9	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	4.1	-3.8	A
I_{DM}	Pulsed Drain Current ²	23	-22	A
EAS	Single Pulse Avalanche Energy ³	16.2	39	mJ
I_{AS}	Avalanche Current	6.8	-6.2	A
$P_D @ T_A = 25^\circ C$	Total Power Dissipation ⁴	1.67	1.67	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	°C
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	75		°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	30		°C/W

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N-Channel Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	40	44	---	V
$\Delta BVDSS/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.032	---	$\text{V}/^{\circ}\text{C}$
RDS(ON)	Static Drain-Source On-Resistance ²	$V_{GS}=10\text{V}$, $I_D=4\text{A}$	---	30	39	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=3\text{A}$	---	40	48	
VGS(th)	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu\text{A}$	1.0	1.7	2.2	V
$\Delta V_{GS(\text{th})}$	$V_{GS(\text{th})}$ Temperature Coefficient		---	-4.5	---	$\text{mV}/^{\circ}\text{C}$
IDSS	Drain-Source Leakage Current	$V_{DS}=32\text{V}$, $V_{GS}=0\text{V}$, $T_J=25^{\circ}\text{C}$	---	---	1	μA
		$V_{DS}=32\text{V}$, $V_{GS}=0\text{V}$, $T_J=55^{\circ}\text{C}$	---	---	5	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=4\text{A}$	---	8	---	S
R _g	Gate Resistance	$V_{DS}=0\text{V}$, $V_{GS}=0\text{V}$, f=1MHz	---	2.4	4.8	Ω
Q _g	Total Gate Charge (4.5V)	$V_{DS}=15\text{V}$, $V_{GS}=4.5\text{V}$, $I_D=3\text{A}$	---	5	---	nC
Qgs	Gate-Source Charge		---	1.54	---	
Qgd	Gate-Drain Charge		---	1.84	---	
Td(on)	Turn-On Delay Time	$V_{DD}=15\text{V}$, $V_{GS}=10\text{V}$, $R_G=3.3\text{k}\Omega$	---	7.8	---	ns
T _r	Rise Time		---	2.1	---	
Td(off)	Turn-Off Delay Time		---	29	---	
T _f	Fall Time		---	2.1	---	
Ciss	Input Capacitance	$V_{DS}=15\text{V}$, $V_{GS}=0\text{V}$, f=1MHz	---	452	---	pF
Coss	Output Capacitance		---	51	---	
Crss	Reverse Transfer Capacitance		---	38	---	
IS	Continuous Source Current ^{1,4}	$V_G=V_D=0\text{V}$, Force Current	---	---	6.3	A
ISM	Pulsed Source Current ^{2,4}		---	---	23	A
VSD	Diode Forward Voltage ²	$V_{GS}=0\text{V}$, $I_S=1\text{A}$, $T_J=25^{\circ}\text{C}$	---	---	1.2	V

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3、The power dissipation is limited by 150°C junction temperature
- 4、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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P-Channel Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=-250\mu\text{A}$	-40	-44	---	V
$\Delta BVDSS/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	-0.018	---	$\text{V}/^{\circ}\text{C}$
RDS(ON)	Static Drain-Source On-Resistance ²	$V_{GS}=-10\text{V}$, $I_D=-3\text{A}$	---	68	77	$\text{m}\Omega$
		$V_{GS}=-4.5\text{V}$, $I_D=-2\text{A}$	---	76	88	
VGS(th)	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=-250\mu\text{A}$	-1.0	-1.7	-2.5	V
$\Delta V_{GS(\text{th})}$	$V_{GS(\text{th})}$ Temperature Coefficient		---	2.5	---	$\text{mV}/^{\circ}\text{C}$
IDSS	Drain-Source Leakage Current	$V_{DS}=-40\text{V}$, $V_{GS}=0\text{V}$, $T_J=25^{\circ}\text{C}$	---	---	-1	uA
		$V_{DS}=-40\text{V}$, $V_{GS}=0\text{V}$, $T_J=55^{\circ}\text{C}$	---	---	-5	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=-5\text{V}$, $I_D=-3\text{A}$	---	5.8	---	S
Qg	Total Gate Charge (-4.5V)	$V_{DS}=-32\text{V}$, $V_{GS}=-4.5\text{V}$, $I_D=-3\text{A}$	---	6.4	---	nC
Qgs	Gate-Source Charge		---	2.1	---	
Qgd	Gate-Drain Charge		---	2.5	---	
Td(on)	Turn-On Delay Time	$V_{DD}=-20\text{V}$, $V_{GS}=-4.5\text{V}$, $R_G=3.3\Omega$, $I_D=-3\text{A}$	---	4.2	---	ns
T _r	Rise Time		---	23	---	
Td(off)	Turn-Off Delay Time		---	26.8	---	
T _f	Fall Time		---	20.6	---	
Ciss	Input Capacitance	$V_{DS}=-15\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	---	620	---	pF
Coss	Output Capacitance		---	65	---	
Crss	Reverse Transfer Capacitance		---	53	---	
IS	Continuous Source Current ^{1,4}	$V_G=V_D=0\text{V}$, Force Current	---	---	-3.8	A
ISM	Pulsed Source Current ^{2,4}		---	---	-22	A
VSD	Diode Forward Voltage ²	$V_{GS}=0\text{V}$, $I_s=-1\text{A}$, $T_J=25^{\circ}\text{C}$	---	---	-1	V

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3、The power dissipation is limited by 150°C junction temperature
- 4、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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N-Typical Characteristics

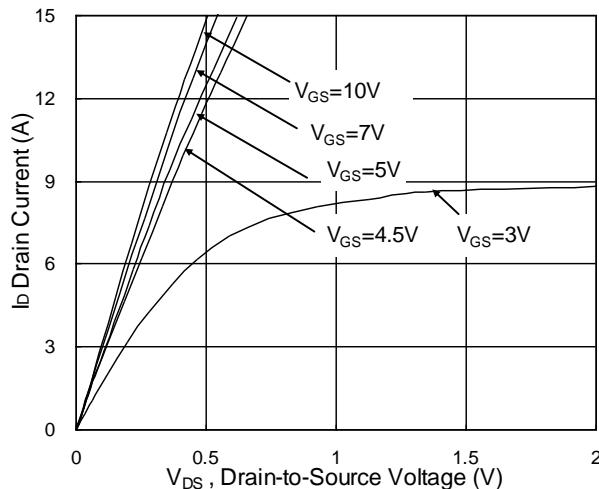


Fig.1 Typical Output Characteristics

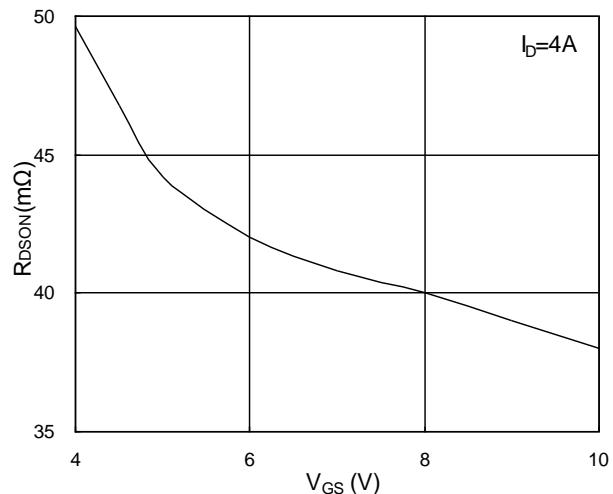


Fig.2 On-Resistance vs. Gate-Source

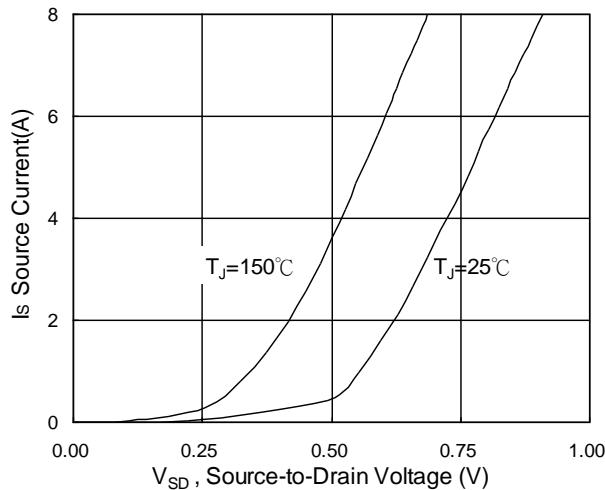


Fig.3 Forward Characteristics Of Reverse

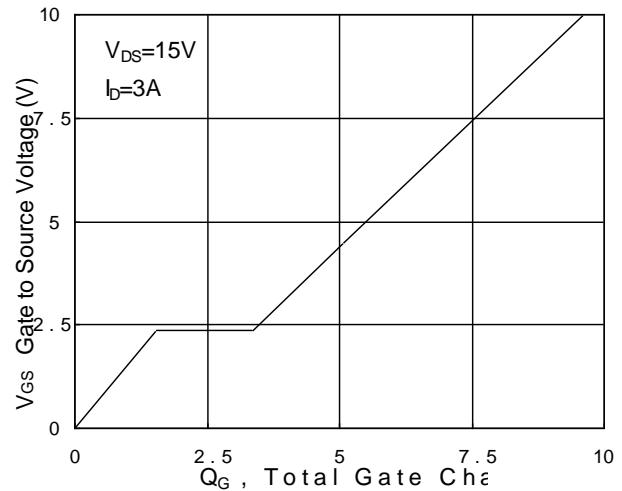


Fig.4 Gate-Charge Characteristics

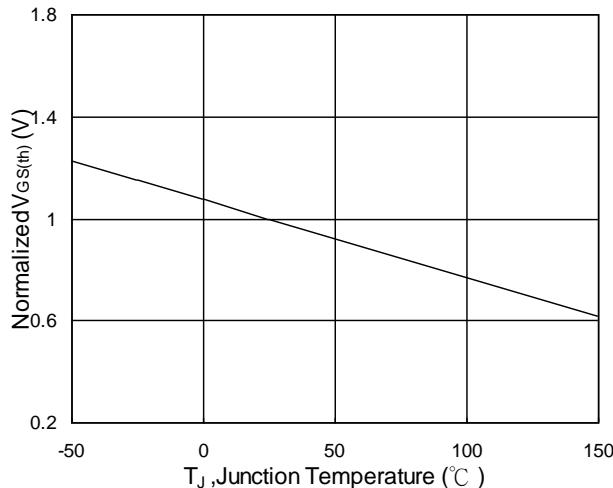


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

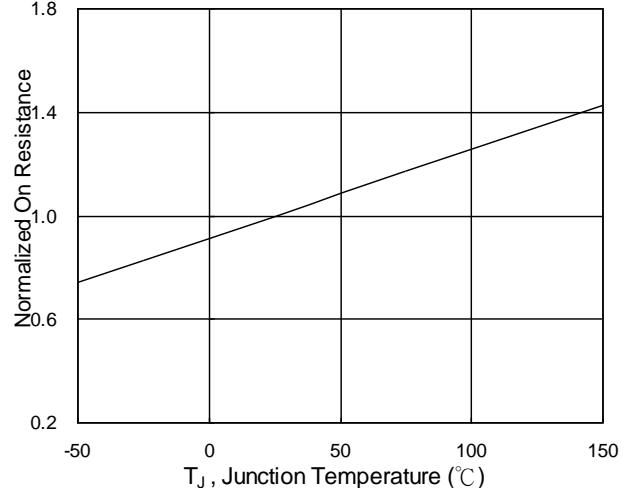
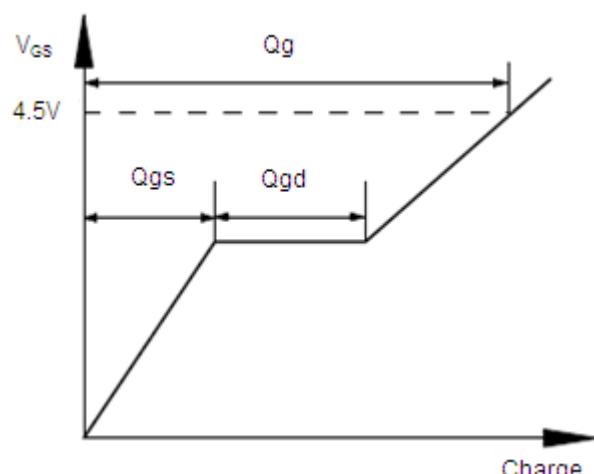
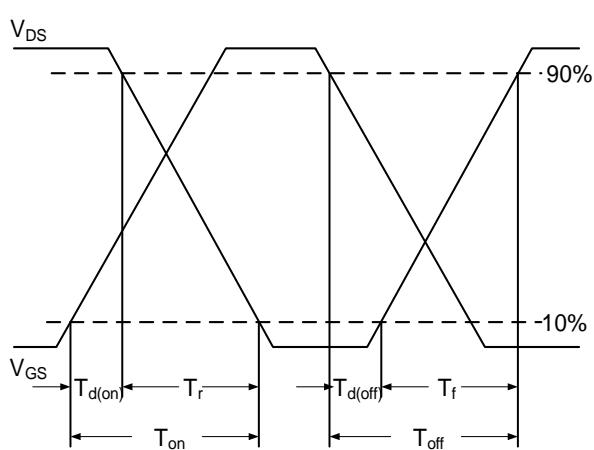
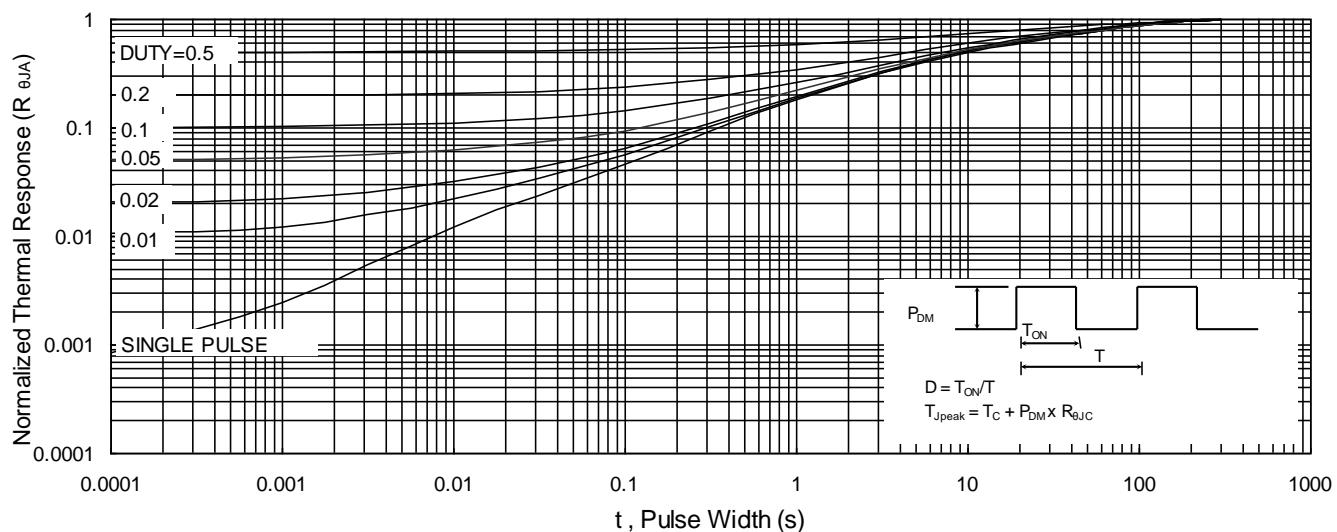
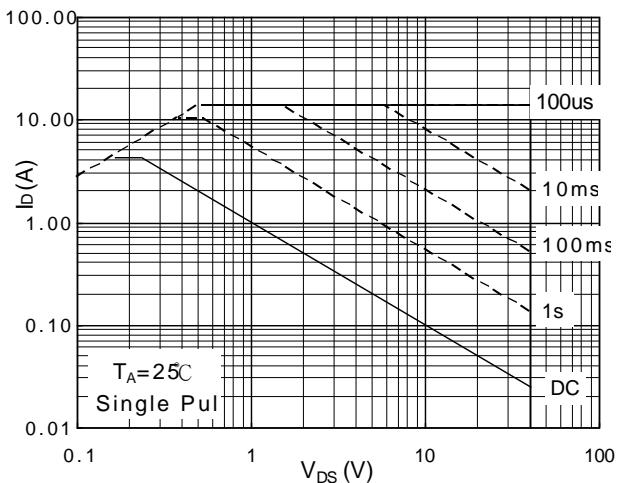
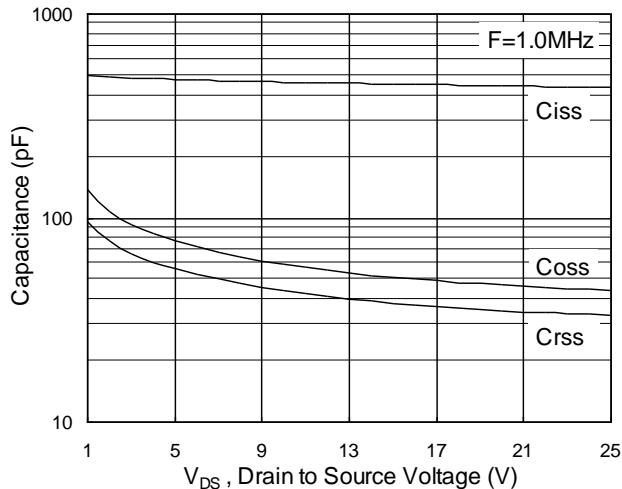


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

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P-Typical Characteristics

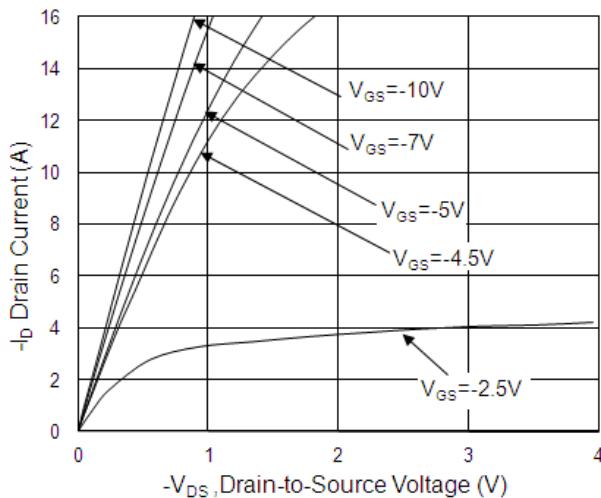


Fig.1 Typical Output Characteristics

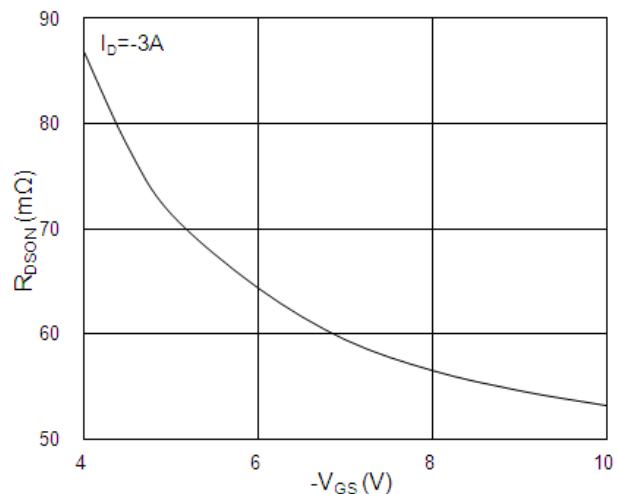


Fig.2 On-Resistance vs. G-S Voltage

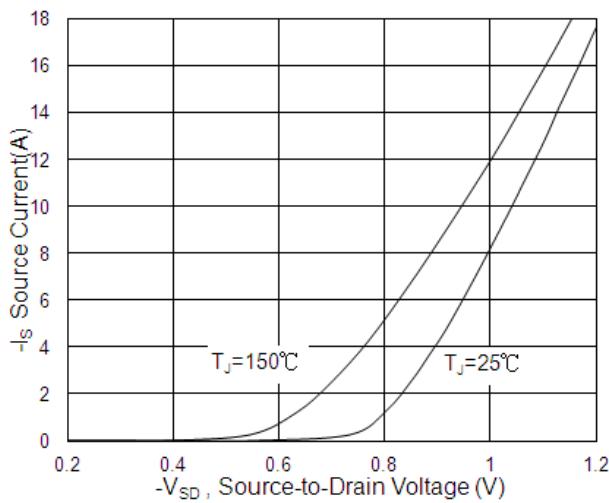


Fig.3 Forward Characteristics Of Reverse

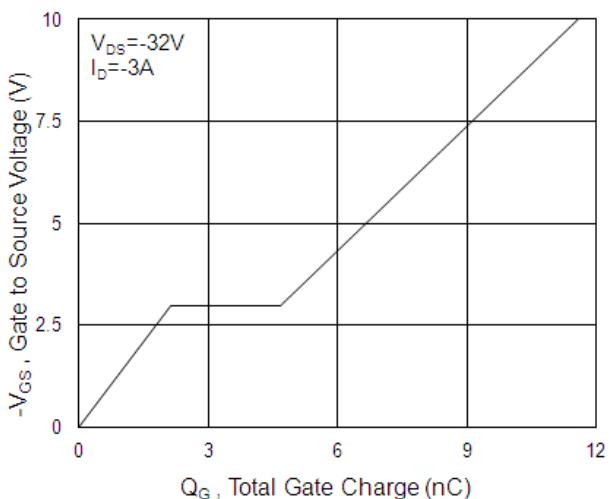


Fig.4 Gate-Charge Characteristics

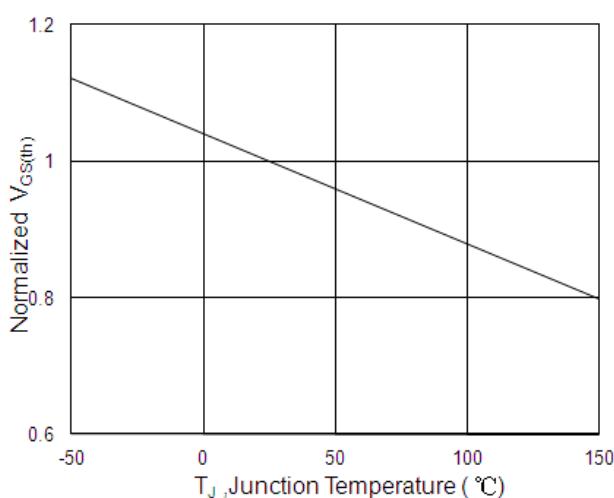


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

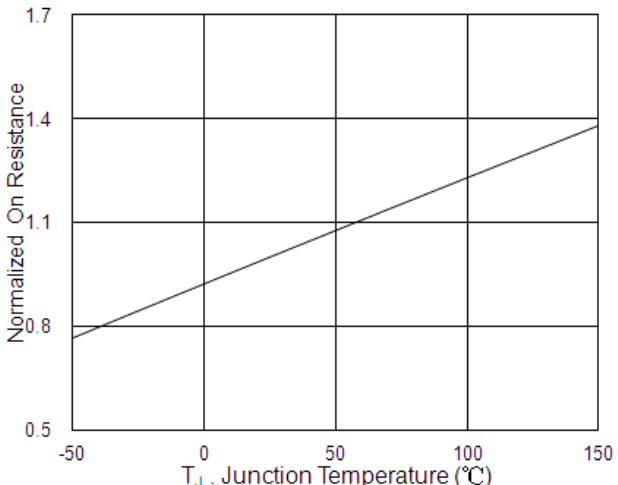


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

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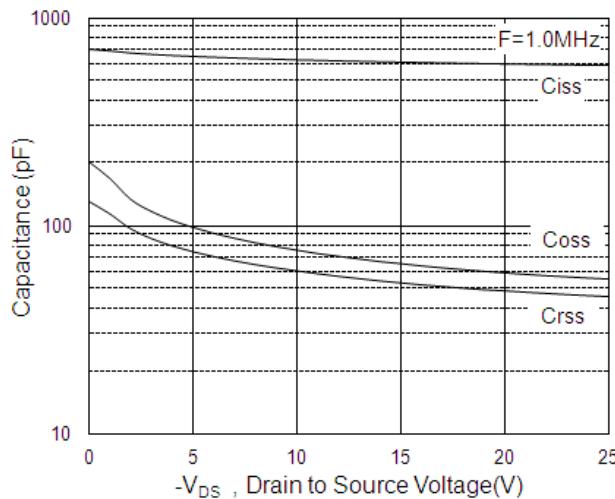


Fig.7 Capacitance

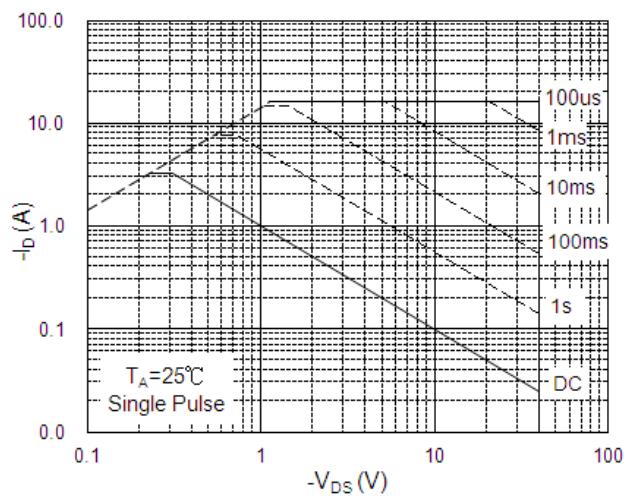


Fig.8 Safe Operating Area

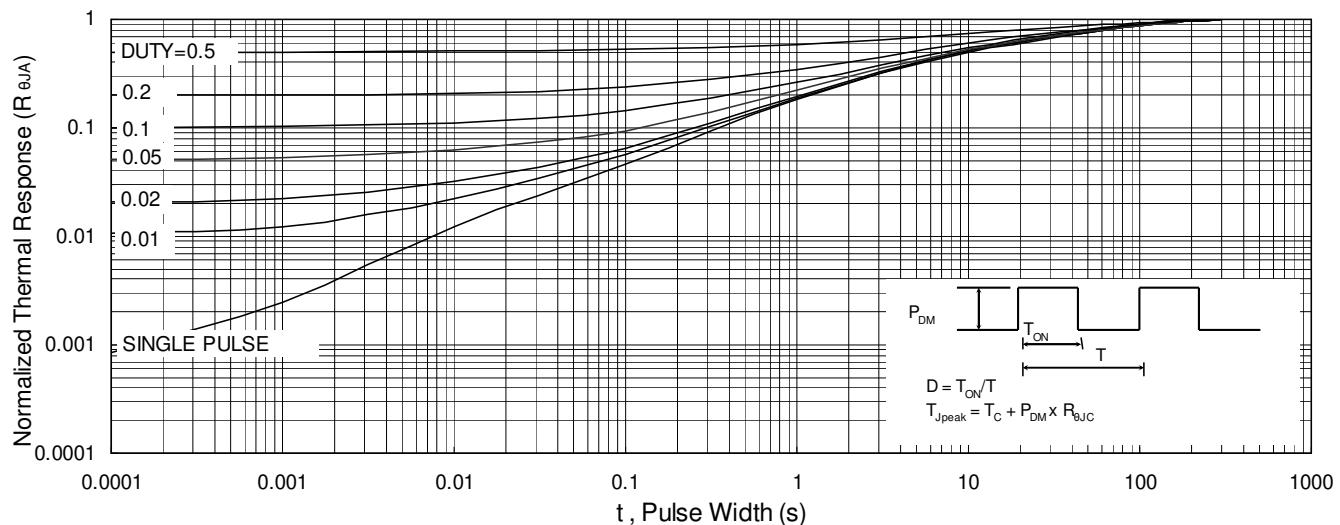


Fig.9 Normalized Maximum Transient Thermal Impedance

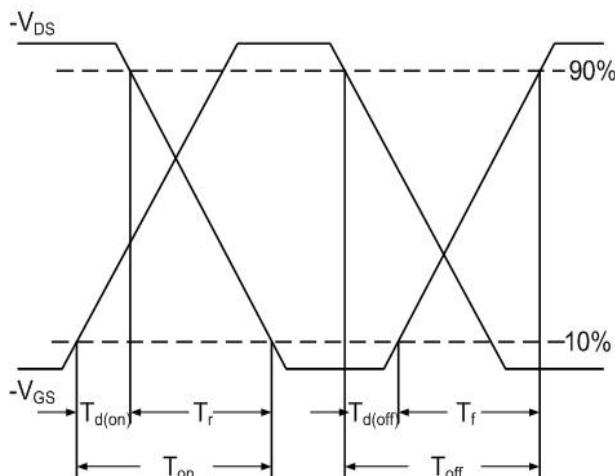


Fig.10 Switching Time Waveform

Data and specifications subject to change without notice.

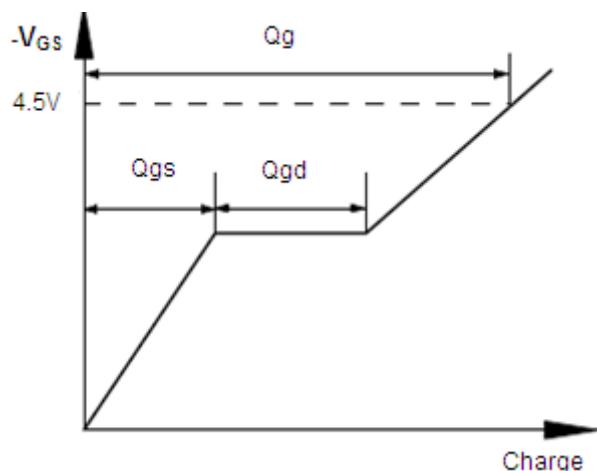
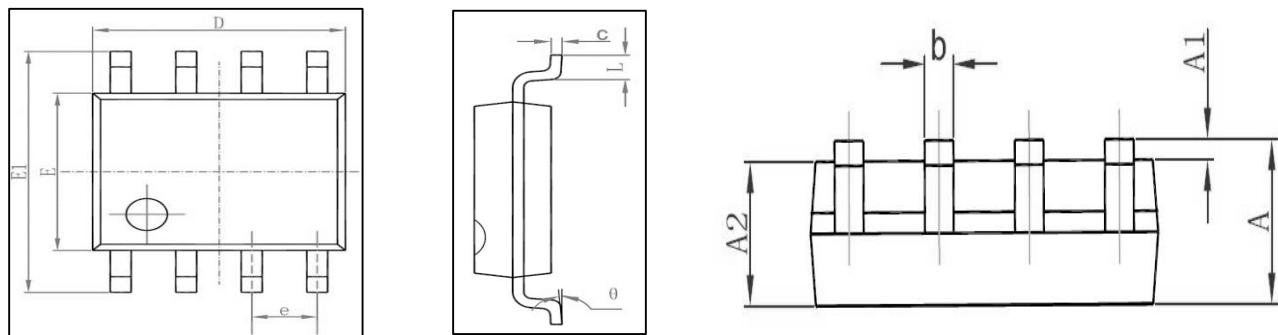
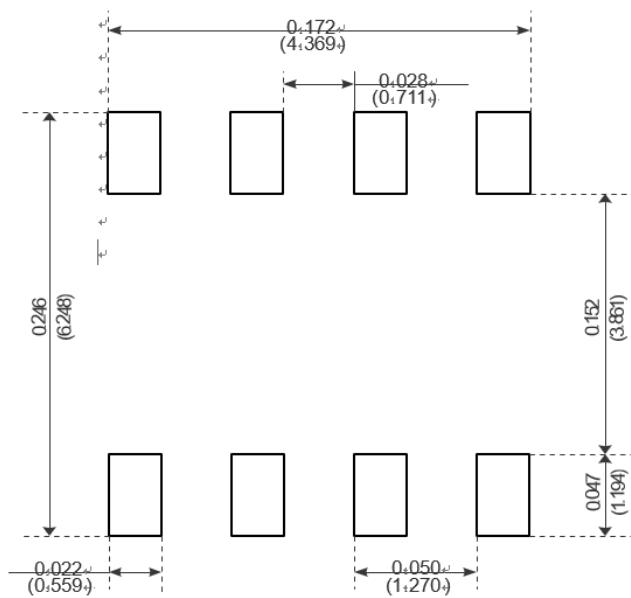


Fig.11 Gate Charge Waveform

Package Mechanical Data:SOP-8L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Recommended Minimum Pads